1. (currently amended) A chip package structure comprising:

a ~~silicon~~ substrate having a surface;

only a die, wherein the die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die is adhered to the surface of the ~~silicon~~ substrate, and the surface of the substrate has an area larger than that of the active surface of the die; and

a thin-film circuit layer located over ~~on top of~~ the ~~silicon~~ substrate and the die and having ~~has~~ an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die.

2. (currently amended) The structure in claim 1, wherein the die has an internal circuitry and a plurality of active devices located on the active surface of the die and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry ~~forms~~ contains the metal pads.

3. (currently amended) The structure in claim 2, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to other ~~one~~ of the active devices via the internal circuitry.

4. (currently amended) The structure in claim 3, wherein a width, length, or ~~and~~ thickness of the traces of the external circuitry is ~~are~~ greater than that of ~~corresponding~~ the traces of the internal circuitry to reduce RC delay.

5. (original) The structure in claim 1, wherein the external circuitry further comprising a power/ground bus.

6. (currently amended) The structure in claim 1, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located over ~~on top of~~ the ~~silicon~~ substrate and the die, and the patterned wiring layer is located over ~~on top of~~ the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

7. (currently amended) The structure in claim 6, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die via ~~by~~ the thru-holes.

8. (currently amended) The structure in claim 6, wherein a via metal is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die via ~~by~~ the via metal ~~vias~~.

9. (currently amended) The structure in claim ~~6~~ 8, wherein the patterned wiring layer and the via metal ~~vias~~ form the external circuitry.

10. (currently amended) The structure of the claim 1 ~~6~~, further comprising at least one passive device positioned inside or on the thin-film circuit layer ~~wherein the external circuitry further comprising at least one passive device~~.

11. (currently amended) The structure in claim 10 ~~6~~, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

12. (currently amended) The structure in claim 10, wherein the passive device is formed, partly or wholely, by a part of the patterned wiring layer.

13. (original) The structure in claim 6, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

14. (currently amended) The structure in claim 1, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the ~~silicon~~ substrate, the patterned wiring layer that is closest to the ~~silicon~~ substrate is electrically connected to the metal pads of the die through the dielectric layer that is closest to the ~~silicon~~ substrate, where the patterned wiring layer that is furthest away from the ~~silicon~~ substrate contains ~~forms~~ the bonding pads.

15. (currently amended) The structure in claim 14, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the ~~silicon~~ substrate is electrically connected to the metal pads of the die through the thru-holes that are closest to the substrate ~~dielectric layer~~.

16. (currently amended) The structure in claim 15, wherein a via metal is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the ~~silicon~~ substrate is electrically connected to the metal pads of the die via ~~by~~ the via metal ~~vias~~ that is closest to the substrate.

17. (currently amended) The structure in claim 16, wherein the patterned wiring layers and the via metal ~~vias~~ form the external circuitry.

Claims 18-20. (canceled)

21. (original) The structure in claim 18, wherein a material of the dielectric layers is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

Claim 22 (canceled)

23. (currently amended) The structure in claim 1, wherein the ~~silicon~~ substrate comprising a silicon layer and a heat conducting layer formed overlapping, a the surface of the ~~silicon~~ substrate is provided by a surface ~~side~~ of the heat conducting layer, which ~~that~~ is closer to ~~further away from~~ the silicon layer, and the silicon layer has at least one opening that penetrates through the silicon layer and is meant ~~used~~ to form an inwardly protruded area, allowing ~~and the backside of~~ the die put into ~~is adhered to a bottom of~~ the inwardly protruded area.

24. (currently amended) The structure in claim 23, wherein a thickness of the silicon layer ~~substrate~~ is approximately equal to a thickness of the die ~~dies~~.

25. (currently amended) The structure in claim 1 further comprising a filling layer located between the a surface of the ~~silicon~~ substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

26. (original) The structure in claim 25, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

27. (original) The structure in claim 1 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

28. (original) The structure in claim 1 further comprising a plurality of bonding points located on the bonding pads.

29. (currently amended) The structure in claim 28, wherein the bonding points are ~~selected from a group consisting of~~ solder balls~~, bumps, and pins~~.

CLAIMS 30-138 ARE CANCELED.

139. (reinstated-formerly claim 22 and currently amended) The structure in claim 1, wherein the ~~silicon~~ substrate further comprises ~~comprising~~ an inwardly protruded area located on the a surface of the ~~silicon~~ substrate, allowing the die put into ~~where the backside of the die is adhered to a bottom of~~ the inwardly protruded area.